Sinolink Technologies

Datasheet

SL3000B Series
High-Performance Bit Error Rate Tester

Create stressed eye diagrams, authentically reproducing real-world signal integrity issues,
Comprehensively enhance the reliability and stability of high-speed links,
ushering in a new era of exceptional high-speed interconnection!

SINOLINK TECHNOLOGIES (BEIJING) CO.,LTD.

Overview

With the rapid development over the past decade in narrow and broad artificial intelligence, data centers, 5G/6G, cloud storage and cloud computing, commercial robotics, and autonomous driving, data has surpassed oil to become the most valuable resource. High-speed transmission is like the highway network connecting cities, indispensable in industrial applications such as consumer electronics. For instance, the signal transmission among all modules within a data center building, between cabinets, and the high-speed data transmission across cities and countries have accelerated from a doubling of speed every 5-6 years two decades ago to a doubling of speed every 2-3 years today.

As the operating speed of digital circuits increases, the signal transmission rates on PCBs, connectors, and backplanes are also getting higher, with serial data communication playing a dominant role in transmission. Mainstream IEEE Ethernet rates now support 25Gbps and 53.125Gbps, with new rates reaching 106Gbps. High-speed buses in consumer electronics like USB3/4/PCIe have signal rates covering the range from 16Gbps to 64Gbps. The serial high-speed interface rates of high-speed FPGAs have surged from 8Gbps to 28Gbps, and DSPs and ADCs/DACs have transitioned from 3Gbps to 25Gbps. To meet the performance and stability requirements of high-speed serial and parallel bus designs, a high-performance Bit Error Rate Tester is needed to verify the performance and margin of the bus link.

A high-speed link consists of three main parts: the TX transmitter, the transmission channel, and the RX receiver. The receiver, which includes complex equalization and signal conditioning, is the most complicated part of testing. A Bit Error Rate Tester (BERT) is an essential instrument for high-speed receiver testing and is the key test equipment to ensure the reliable operation of the entire link. It can perform stress tests on high-speed receivers from a signal integrity perspective by using the BERT's Pattern Generator (PPG) to inject sinusoidal jitter, random jitter, crosstalk-induced jitter, common-mode noise, differential-mode noise, and broadband white noise to simulate the most severe real-world environments.

The SL3000B series High-Performance Bit Error Rate Tester features excellent performance metrics, a rich set of functions, flexible option configurations, and an extremely high level of integration. It provides powerful performance and a wealth of advanced features for the pre-research, design, and production testing of high-speed serial circuit products. The BERT can test and analyze the bit error rate in high-speed wired communication systems and is primarily used to evaluate the performance of electronic channels. It is an essential instrument for the R&D and testing of high-speed communication hardware circuits, widely used in universities, research institutes, communication equipment R&D, and aerospace research fields.

Features of SL3000B Series High-Performance Bit Error Rate Tester

Powerful modular design

- **A single chassis supports 6 expandable functional slots for flexible configuration of different modules.**
- **Each channel supports rates from 1 GBaud up to 32.4 GBaud, continuously adjustable without gaps.**
- **Supports all mainstream NRZ/PAM4 rates and various non-standard rates up to 32.4 GBaud, with different options available for future rate expansion and upgrades.**
- **A high-speed signal integrity test system with customizable fixtures, matching cables, adapters, etc., to meet the testing needs of different scenarios, creating specialized test tools to make testing more profes sional and simpler.**

Excellent signal integrity and a wealth of advanced features

- **Supports NRZ and PAM4 encoded signaling formats.**
- **The only high-end benchtop BERT in the country that supports mainstream protocol compliance testing, simulating complex real-world environments through a rich injection of low-frequency and high-frequency jitter.**
  - Sinusoidal Jitter (SJ) injection
  - Bounded Uncorrelated Jitter (BUJ) injection
  - Random Jitter (RJ) injection
  - Periodic Jitter (PJ) injection
  - Spread Spectrum Clocking (SSC) injection
  - External Jitter injection
- **Rich variety of noise injections**
  - Common-Mode Noise (CMI) injection
  - Differential-Mode Noise (DMI) injection
  - Broadband Noise (BBN) injection
- **PPG has a built-in 4-tap FFE, providing flexible pre-distortion settings for channel compensation.**
- **PPG supports high-voltage differential output up to 1.8V.**
- **PPG supports adjustable rise time for different rates.**
- **PPG supports phase/skew adjustment between multiple channels with up to picosecond resolution.**
- **PPG supports multiple random patterns and the industry's most advanced custom patterns.**
  - PRBS random patterns, high/medium/low-frequency clock patterns.
  - User-defined patterns of ⩾16 Gbit
- **The receiver (ED) supports advanced automatic equalization to easily meet various complex test environments.**
- **The receiver (ED) has a built-in Clock Data Recovery (CDR) function, eliminating the need for an external clock input.**

Rich test-related information

The RX receiver is the final stage of the entire high-speed link. Receiver testing is challenging because it is internal to the chip, making it impossible to directly observe signal integrity issues in most scenarios. The most mainstream method is to create a stressed eye to simulate the most demanding real-world operating conditions. The BERT is the core test instrument for constructing and calibrating this stressed eye. For a high-speed transmission link, the receiver must be able to reliably receive transmitted data under the most severe conditions. Various signal integrity issues at the transmitter and along the link can degrade the signal and reduce the receiver's margin. The SL3000B series BERT provides the most comprehensive RX receiver stressed eye test solution, capable of injecting up to 10 different types of jitter, noise, and other signal integrity impairments to simulate the most severe and complex real-world environments.

Applications of SL3000B Series High-Performance Bit Error Rate Tester

As the operating speeds of digital circuits increase, the signal transmission rates on PCBs, connectors, and backplanes are also getting higher, with serial data communication playing a dominant role. Precision-designed high-speed interconnects such as PCIe/ETH/VPX backplanes and high-speed cables, designed to the strictest performance standards, have become crucial in the current context of widespread demand for high-speed signals in national defense. The backplane is the communication backbone in embedded systems and must be designed according to strict signal integrity standards to ensure timely and accurate data transmission between modules within the system. As systems move towards supporting higher serial bit rates like 100G-baseKR4/CR4 and PCIe Gen4/5 protocols, high signal integrity is essential for achieving fail-safe operation. To meet the performance expectations of high-speed transmission, especially for high-speed receivers, receiver tolerance testing is crucial.

Typical applications

Additionally, mainstream high-speed IEEE Ethernet rates have increased from 10Gbps to support 25Gbps and 53Gbps. High-speed buses in consumer electronics like PCIe and USB3/4 now cover signal rates from 2.5Gbps to 20Gbps. The serial high-speed interface rates of high-speed FPGAs have surged from 8Gbps to 28Gbps, and DSPs and ADCs/DACs have transitioned from 3Gbps to 32Gbps. The SL3000B series High-Performance Bit Error Rate Tester can perform receiver tolerance testing for various high-speed standard protocols and non-standard rates

- **High-speed interconnect signal integrity testing.**
- **Receiver tolerance and margin testing for high-speed interfaces of high-speed chips such as SERDES/FPGA/DAC/ADC.**
- **R&D testing for high-speed data centers, optical communications, and optical modules.**
- **R&D testing for laser communications and coherent optics.**
- **Pre-compliance physical layer testing for various high-speed standard and non-standard buses.**

Specifications of SL3000B Series High-Performance Bit Error Rate Teste

Mainframe SL3004B Specifications

General Specifications

External Display Interface	HDMI
USB Interface	4 x USB 2.0
Module Slots	6
Grounding Terminal	1 on front panel 1 on rear panel
Operating System	Windows Server 2019
Storage Capacity	256GB
Remote Interface	Ethernet
Environmental Parameters	
Power Supply	100V to 240Vac
Power Consumption	⩽ 1000W
Operating Temperature	+10°C to +40°C
Storage Temperature	-20°C to +70°C
Operating Humidity	Non-condensing, +35°C, 20% to 80%
Dimensions & Weight	Dimensions: 440mm × 529mm × 177mm (WidthDepthHeight) Weight: ⩽35KG

PPG Pattern Generator SL311321B / SL311322B Specifications

PPG Operating Rate

Rate Range	NRZ/PAM4: 1 GBaud - 32.4 GBaud continuously adjustable
Rate Step	1 kBaud
Clock Frequency Range	1 GHz to 16.2 GHz

PPG Output Equalization

De-emphasis Taps	4-tap equalization control (2 post-cursor, 1 pre-cursor, 1 main)
Setting Range	PPGEQ Standard: Post-Cursor1: –6 to +7.5dB, 0.1 dB step Post-Cursor2: –3 to +3 dB, 0.1 dB step Pre-Cursor1: –6 to +6dB, 0.1 dB step -9dB Option: Post-Cursor1: –9 to +9 dB, 0.1 dB step Post-Cursor2: –9 to +9 dB, 0.1 dB step Pre-Cursor: –9 to +9dB, 0.1 dB step
Accuracy	±1.5dB (typ)

PPG Data Output

Number of Output Channels	1 / 2 channels
Output Amplitude	
Setting Range	100mV to 1200mV (differential), 10mV settable step.
High Voltage Option (-1P8V)	Extends up to 1800mV (differential), 10mV settable step.
Output Error	±80mV ±17%
DC Offset (Option)	±1V, 4mV settable step
Setting Error	±85 mV ±10% offset voltage
Output Amplitude Protection	Supports preset maximum amplitude limit (LEVEL Guard)
External Attenuation Auto Compensation	-40dB to 0dB, 0.2dB step
Rise/Fall Time (20% to 80%)	14ps (typ, NRZ@25.78125Gbps)
Random Jitter	<150 fs, RMS (typ, 25.78125Gbps); in spectrum analyzer phase noise mode with frequency offset from 10kHz to 100MHz
Crossing Point	
Setting Range	42% to 58%, 0.5% settable step
Setting Error	±2%
Termination	AC/DC
Connector	2.92mm (f)

PPG Output Pattern

Output Pattern	Random Patterns: PRBS7/9/13/15/23/31/PRBS13Q/PRBS31Q Others:JP03A/JP03B/ SSPRQ
Custom Pattern	
Data Length	Standard: 128-bit custom pattern Custom Pattern Extension Option supports 128 bit/8 Mbit/256 Mbit/4 Gbit/16 Gbit
Signaling Encoding	NRZ/ PAM4
NRZ	Positive polarity / Negative polarity
PAM4 Gray Code	Supported

PPG Jitter Injection

Low-Frequency Sinusoidal Jitter (LFSJ1/LFSJ2)	2 independent Low-Frequency Sinusoidal Jitter (LFSJ) injections Standard: Frequency Range: 1kHz to 10MHz Amplitude Range: @16Gbps 1kHz: 2000UI 10kHz: 200UI 100kHz: 20UI 1MHz: 2UI 10MHz: 0.4UI
High-Frequency Periodic Jitter (HFPJ1/HFPJ2)	2 independent High-Frequency Periodic Jitter (HFPJ) injections: Standard: Frequency Range: 1MHz to 100MHz Amplitude Range: 1MHz: 0.3UI 10MHz: 0.3UI 100MHz: 0.3UI High-Frequency Jitter (HFSJ) Extension Option: Frequency Range: 100MHz to 250MHz Amplitude Range: 100MHz: 0.3UI 150MHz: 0.3UI 250MHz: 0.3UI Note: Actual JTOL (Jitter Tolerance) testing includes other jitter components such as RJ, BUJ, etc., in addition to SJ/PJ.
Spread Spectrum Clocking (SSC)	Frequency Range: 28kHz to 37kHz Modulation Profile: Down-spread / Center-spread / Up-spread Frequency Deviation: 1Gbps to 16Gbps: 0 to 5500ppm; 16Gbps to 32Gbps: 0 to 4900ppm Accuracy: ±200 ppm
Random Jitter (RJ)	Amplitude Range: 0-250mUI (pk-pk), Q≈14 Accuracy: ±4 ps ±15% High-Pass Filter: 10MHz, 20MHz, Through Low-Pass Filter: 100MHz, 500MHz, 1GHz, Through
Bounded Uncorrelated Jitter (BUJ)	Bit Rate Range: 500Mbps to 10Gbps Pattern: PRBS7, 9, 15, 20, 23, 29, 31 Amplitude Range: 0-280mUI (pk-pk) Accuracy: ±4 ps ±15% (Jitter clock output frequency ⩾ 4GHz); ±7 ps ±15% (Jitter clock output frequency < 4GHz) Low-Pass Filter: 50MHz 3rd-order, 100MHz 3rd-order, 200MHz 3rd-order, Through

PPG Inter-Channel Delay Adjustment

Bit Shift Adjustment	-128 to +127, delay adjustment in bit units (Bit shift)
Fine Skew Adjustment	1UI, Skew adjustment resolution ⩽1.5ps
Termination	AC, 50Ω
Connector	2.92mm (f)

PPG Data Output Rise Time Adjustment

Rise Time (20%~80%	14ps (typ, NRZ@25.78125Gbps)

PPG Clock Outpu

Half-Rate Clock	1GHz to 16.2GHz
Number of Channels	1
Termination	AC,50Ω
Connector	SMA (f)

PPG External Clock Input

Number of Input Ports	1 (single-ended)
Input Frequency Range	Input Amplitude
Input Amplitude	-5dBm to +5dBm
Termination	AC,50Ω
Connector	SMA (f)

PPG NRZ Mode Error Injection

Error Injection Region	ALL
Internal Trigger	
Error Injection Mode	Repeat / Single
Error Rate	E-n (=1 to 9, n=3 to 12)

PPG PAM4 Mode Error Injection

Type	MSB error injection, LSB error injection, MSB and LSB error injection
MSB Error Injection	
Error Injection Mode	Repeat / Single
Error Rate	E-n (=1 to 9, n=3 to 12)
LSB Error Injection	
Error Injection Mode	Repeat / Single
Error Rate	E-n (=1 to 9, n=3 to 12)
MSB and LSB Error Injection	
Error Injection Mode	Repeat / Single
Error Rate	E-n (=1 to 9, n=3 to 12)

High-Speed Clock Source Module SL361164B Specifications

SL361164B 16GHz Frequency Synthesizer with Jitter

External Jitter Input	Number of Channels: 1 Frequency Range: 10kHz to 1GHz Connector: SMA (f)
Jittered Clock Output	Number of Channels: 4 Frequency Range: 1GHz to 16.2GHz Output Power: 0dBm ± 5dB Frequency Offset: ⩾±0.5 ppm Connector: SMA (f)
Sub-rate Clock Output	Number of Channels: 1 Frequency Range: 1/n clock (n range is: (1 to 127) * (1/2/4/8)) Connector: SMA (f)
JIT Option	
Low-Frequency Sinusoidal Jitter (LFSJ1/LFSJ2)	2 independent Low-Frequency Sinusoidal Jitter (LFSJ) injections Frequency Range: 1KHz to 10MHz Amplitude Range: 1KHz: 1000UI 10KHz: 200UI 100KHz: 20UI 1MHz: 1.2UI 10MHz: 1UI
High-Frequency Periodic Jitter (HFPJ1/HFPJ2)	2 independent High-Frequency Periodic Jitter (HFPJ) injections: Standard: Frequency Range: 1MHz to 100MHz Amplitude Range: 1MHz: 0.3UI 10MHz: 0.3UI 100MHz: 0.3UI High-Frequency Jitter (HFSJ) Extension Option: Frequency Range: 100MHz to 250MHz Amplitude Range: 100MHz: 0.3UI 150MHz: 0.3UI 250MHz: 0.3UI Note: Actual JTOL (Jitter Tolerance) testing includes other jitter components such as RJ, BUJ, etc., in addition to SJ/PJ.
Random Jitter (RJ)	Amplitude Range: 0-250mUI (pk-pk), Q≈14 Accuracy: ±4 ps ±15% High-Pass Filter: 10MHz, 20MHz, Through Low-Pass Filter: 100MHz, 500MHz, 1GHz, Through
Bounded Uncorrelated Jitter (BUJ)	Bit Rate Range: 500Mbps to 10Gbps Pattern: PRBS7, 9, 15, 20, 23, 29, 31 Amplitude Range: 0-280mUI (pk-pk) Accuracy: ±4 ps ±15% (Jitter clock output frequency ⩾ 4GHz); ±7 ps ±15% (Jitter clock output frequency < 4GHz) Low-Pass Filter: 50MHz 3rd-order, 100MHz 3rd-order, 200MHz 3rd-order, Through
-SSC Option	
Spread Spectrum Clocking (SSC)	Frequency Range: 28kHz to 37kHz Modulation Profile: Down-spread / Center-spread / Up-spread Frequency Deviation: 0 to 5500ppm Accuracy: ±100 ppm

ED Error Detector SL32001B / SL32002B / SL32004B Specifications

Noise Injection SL35001B Module Specifications Error Detector

ED Operating Rate

Operating Rate	1.25Gbps to 32.4Gbps, NRZ

ED Pattern

Input Pattern	PRBS7/9/13/15/23/31
Custom Pattern	
Data Length	Not supported

ED System Clock

Clock Recovery	Built-in clock recovery

Note: Only supports clock recovery, does not support external clock.

ED Data Input

Number of Input Channels	1/2/4 channels selectable
Input Signal Format	NRZ
Input Amplitude	100mVppd to 1200mV ppd
Input Sensitivity	80mVd differential eye height
Termination	DC,50Ω
Connector	2.92mm（f）
CTLE	Supported (fixed equalization)
Clock Recovery	Supported

Noise Injection SL351321B/SL351322B Module Specifications

Common-Mode Noise (CMI) Option

Frequency	
Range	100MHz to 6GHz
Step	1MHz
Accuracy	⩽ ±1MHz
Amplitude	
Setting Range	10mVpp to 250mVpp
Step	10mVpp
Accuracy	±20%±25mVpp
Waveform	Sine
Setting Status	
Manual	Amplitude and frequency independently adjustable
PCIe3	Amplitude: 100mVpp Frequency: 400MHz
PCIe4	Amplitude: 150mVpp Frequency: 120MHz
PCIe5	Amplitude: 150mVpp Frequency: 120MHz

Differential-Mode Noise (DMI) Option

Frequency	
Range	2GHz to 10GHz
Step	10MHz
Accuracy	⩽ ±1MHz
Amplitude	
Setting Range	5mVpp to 100mVpp
Step	5mVpp
Accuracy	±20%±10mVpp
Waveform	Sine
Setting Status	
Manual	Amplitude and frequency independently adjustable
PCIe3	Amplitude: 16mVpp Frequency: 2.1GHz
PCIe4	Amplitude: 16mVpp Frequency: 2.1GHz
PCIe5	Amplitude: 10mVp Frequency: 2.1GHz

Broadband White Noise Option

Frequency	
Range	10MHz to 16GHz
Amplitude	
Setting Range	0.2mVrms to 25mVrms
Step	0.2mVrms
Crest Factor	＞ 5pp/rms
Flatness	±7dB

SL3000B High-Speed Bit Error Rate Tester Configuration and Selection Guide

SL3000B High-Speed Test Accessories

SL3000B Series High-Performance Bit Error Rate Tester Accessories	
SL-Monitor156	Configure a separate 15-inch display
SL-ISI	ISI variable insertion loss channel board
SL-XTALK	Signal integrity impairment board
SL-SW-Datalink-Insight	High-speed signal integrity analysis toolkit Datalink-Insight
SL-400G QSFP-DD MCB	400G QSFP-DD MCB test fixture
SL-100G QSFP28 MCB	100G QSFP28 MCB test fixture
SL-SFP28 MCB	SFP28 MCB test fixture
SL-Fixture-Cus	Custom designed test fixture (Please contact Sinolink to discuss technical details)
SL-292mm-m2m-12	2.92mm cable assembly (male to male with 12inch)
SL-292mm-m2m-24	2.92mm cable assembly (male to male with 24inch)
SL-24mm-m2m-12	2.4mm cable assembly (male to male with 12inch)
SL-24mm-m2m-24	2.4mm cable assembly (male to male with 24inch)
SL-185mm-m2m-12	1.85mm cable assembly (male to male with 12inch)
SL-185mm-m2m-24	1.85mm cable assembly (male to male with 24inch)
SL-292mm-m2m	2.92mm male to male connector
SL-292mm-f2f	2.92mm female to female connector
SL-24mm-m2m	2.4mm male to male connector
SL-24mm-f2f	2.4mm female to female connector
SL-185mm-m2m	1.85mm male to male connector
SL-185mm-f2f	1.85mm female to female connector
SL-292m-24f	2.92mm male to 2.4mm female connector
SL-292f-24m	2.92mm female to 2.4mm male connector
SL-Term-50	50ohm termination
SL-LTW-08090	Torque wrench
SL-HTC	Reinforced packing case

Warranty Service

SL3000B Series Bit Error Rate Tester Warranty	
Standard	1-year warranty and support for the mainframe plus all ordered modules
SL-W3	3-year warranty and support option for the mainframe plus all ordered modules
SL-W5	5-year warranty and support option for the mainframe plus all ordered modules

Sinolink Technologies (Beijing) Co., Ltd., founded in 2009, has long focused on the research and development of high-frequency, high-rate, ultra high bandwidth, and measurement technologies. It provides stable, reliable, and high-performance dedicated test and measurement software and hardware tools for traditional application fields such as satellite communications, radar, and complex electromagnetic environments, as well as emerging industries like 5G mobile communications and high-speed interconnects.

Sinolink Technologies is a national high-tech enterprise, a national-level "Little Giant" enterprise for specialized and innovative SMEs, a Beijing municipal enterprise technology research and development institution, a council member of the China Electronic Instrument Industry Association, a member of the China Machinery Industry Federation, and a council member of the China Electromagnetic Environment Effects Industry Technology Innovation Strategic Alliance. Its products with independent intellectual property rights are widely used in government R&D, corporate R&D, and higher education institutions, serving over 200 domestic and international clients annually, with a cumulative total of thousands of clients served. It is one of the leading suppliers of high-end R&D instruments in China's electronic measurement field and a leader in certain niche application areas.

Focus achieves professionalism; innovation serves applications. Sinolink Technologies has a deep understanding of industry applications. Relying on traditional test and measurement theories and technologies, and collaborating with industry-leading elites, we are committed to improving the practicality, convenience, and cost-effectiveness of test tools, helping engineers to devote more time and energy to R&D and production itself. Through innovative test solutions, we accelerate technological development in related fields, drive the iteration and renewal of the industries we serve, and contribute to the progress of human civilization.

Sinolink Technologies

For more information on the products, applications and services of Sinolink Technologies (Beijing) Co.,Ltd please visit: www.sinolink-technologies.com

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1-Year Warranty
The combination of superior product reliability and 1-year warranty service helps you achieve the following goals: increased measurement confidence, reduced cost of

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